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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,857	02/22/2002	Jingkuang Chen	111517	4718

27074 7590 07/27/2004

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EXAMINER	
HOGANS, DAVID L	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,857	CHEN ET AL.	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *29-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Supplemental Response filed on April 27, 2004.

Status of Claims

Claims 1-16 are pending. Claims 29-38 are withdrawn. Claims 17-28 and 39-46 are cancelled.

Election/Restrictions

As to the arguments put forth by the Applicant in the Remarks filed on February 5, 2004, the Examiner kindly refers Applicant to the December 31, 2003, Non-Final Rejection wherein the Requirement for Restriction was held to be final.

Finally, the Applicant requests rejoinder of Claims 29-38. The Examiner is uncertain as to the basis for this request. It appears that neither MPEP § 809 nor MPEP § 821 provides a basis for such a request.

Specification

The objection to the specification has been withdrawn pursuant to Applicant's amendments.

Claim Rejections - 35 USC § 112

The rejection of Claims 13-16 and 14-16 under 35 USC § 112, first paragraph, has been withdrawn pursuant to Applicant's amendments.

The rejection of Claims 8-16 under 35 USC § 112, second paragraph, has been withdrawn pursuant to Applicant's amendments.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 4-5 are rejected under 35 U.S.C. 102(b) as being anticipated by 5,498,554 to Mei.

In reference to Claims 1, 4 and 5, Mei teaches:

- providing a p-type silicon substrate (10); (See Figures 2 and 3, columns 2-10 lines 45-45 and Tables A and B – noting alternate examples in Table B)
- forming a first protective layer (220) over the substrate; (See Figures 2 and 3, columns 2-10 lines 45-45 and Tables A and B)
- removing a portion of the first protective layer to expose a first portion of the substrate; (See Figures 2 and 3, columns 2-10 lines 45-45 and Tables A and B)
- ion implanting a high voltage well (40A or 40B) of a first circuit device in the first portion of the substrate using the partially removed first protective layer; (See Figures 2 and 3, columns 2-10 lines 45-45 and Tables A and B)
- forming a second protective layer (230C) over at least the first portion of the substrate; (See Figures 2 and 3, columns 2-10 lines 45-45 and Tables A and B)

- removing a second portion of the first protective layer to expose a second portion of the substrate; (See Figures 2 and 3, columns 2-10 lines 45-45 and Tables A and B) and
- ion implanting a first low voltage well (60A) of a second circuit device in the second portion of the substrate using the partially removed first protective layer (220) and the second protective layer (230C) (See Figures 2 and 3, columns 2-10 lines 45-45 and Tables A and B)

The Examiner notes that "ion implanting a high voltage well" or "ion implanting a first low voltage well" does not necessarily mean forming a high or low voltage well. One can ion implant a high voltage well or a low voltage well by merely implanting a channel stop or a tank region within the high/low voltage well.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 4-5 and 8-13 are rejected under 35 U.S.C. 102(e) as being anticipated by 6,686,233 to Soderbarg et al.

In reference to Claims 1, 4 and 5, Soderbarg et al. teaches:

- providing a p-type silicon substrate (1); (See Figures 1-12 and columns 3-7 lines 65-45)
- forming a first protective layer (5 or 11) over the substrate; (See Figures 1-12 and columns 3-7 lines 65-45)
- removing a portion of the first protective layer to expose a first portion (7 or 9) of the substrate; (See Figures 1-12 and columns 3-7 lines 65-45)
- ion implanting a high voltage well (7 or 9) of a first circuit device in the first portion of the substrate using the partially removed first protective layer; (See Figures 1-12 and columns 3-7 lines 65-45)
- forming a second protective layer (13) over at least the first portion of the substrate (7 or 9); (See Figures 1-12 and columns 3-7 lines 65-45)
- removing a second portion of the first protective layer (15) to expose a second portion of the substrate; (See Figures 1-12 and columns 3-7 lines 65-45) and
- ion implanting a first low voltage well (17) of a second circuit device in the second portion of the substrate using the partially removed first protective layer (5 or 11) and the second protective layer (13) (See Figures 1-12 and columns 3-7 lines 65-45)

The Examiner notes that "ion implanting a high voltage well" or "ion implanting a first low voltage well" does not necessarily mean forming a high or low voltage well. One can

ion implant a high voltage well or a low voltage well by merely implanting a channel stop or a tank region within the high/low voltage well.

In reference to Claim 8, Soderbarg et al. teaches:

- forming a third protective layer (37) over the substrate; (See Figures 1-12 and columns 3-7 lines 65-45)
- removing a portion of the third protective layer; (See Figures 1-12 and columns 3-7 lines 65-45) and
- ion implanting a second low voltage well (39 or 41) of the second circuit device in the substrate (See Figures 1-12 and columns 3-7 lines 65-45)

The Examiner notes that "ion implanting a second low voltage well" does not necessarily mean forming a second low voltage well. One can ion implant a low voltage well by merely implanting a channel stop, a tank region or a source/drain region within the low voltage well.

In reference to Claim 9, Soderbarg et al. teaches:

- forming a field oxide layer (19) over at least part of each of the high voltage well, the first low voltage well and the second low voltage well (See Figures 1-12 and columns 3-7 lines 65-45)

In reference to Claim 10, Soderbarg et al. teaches:

- ion implanting the substrate to adjust a threshold (23) of the high voltage well, the first low voltage well and the second low voltage well (See Figures 1-12 and columns 3-7 lines 65-45 - noting Figure 6)

In reference to Claim 11, Soderbarg et al. teaches:

- forming a polysilicon layer (25, 27 and 29) over a gate oxide (21) and the field oxide layer (19); and removing a portion of the polysilicon layer to define a polysilicon gate for each of the high voltage well (25), the first low voltage well (27) and the second low voltage well (29) (See Figures 1-12 and columns 3-7 lines 65-45)

In reference to Claim 12, Soderbarg et al. teaches:

- forming a fourth protective layer (33) over at least the field oxide layer (19) and the polysilicon gates (25, 27 and 29); (See Figures 1-12 and columns 3-7 lines 65-45)
- removing a portion of the fourth protective layer; (See Figures 1-12 and columns 3-7 lines 65-45) and
- ion implanting a P-body (31) in the high voltage well of the first circuit device using the partially removed fourth protective layer (See Figures 1-12 and columns 3-7 lines 65-45)

In reference to Claim 13, Soderbarg et al. teaches:

- forming a fifth protective layer (43) over at least the field oxide layer (19) and the polysilicon gates (29); (See Figures 1-12 and columns 3-7 lines 65-45)
- removing a portion of the fifth protective layer; (See Figures 1-12 and columns 3-7 lines 65-45) and
- ion implanting at least one N+ source/drain (49) in the P-body (31), in the high voltage well of the first circuit device and in the first low voltage well (45 and 47) of the second circuit device using the partially removed fifth protective layer (See Figures 1-12 and columns 3-7 lines 65-45)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,498,554 to Mei in view of 5,519,247 to Arbus et al.

Incorporating all arguments of Claim 1 and noting that Mei fails to explicitly teach ion implanting a photodiode into the substrate.

However, Arbus et al., in Figure 1a and columns 2-5 lines 19-29, teaches a photodiode implanted into a substrate with CMOS and DMOS technology (i.e. – low and high voltage well implants).

It would have been obvious to one of ordinary skill in the art to modify Mei by incorporating a photodiode implanted into a substrate with CMOS and DMOS technology, as taught by Arbus et al., to place the amplifier circuits near the photodiode and consequently increase the speed of action of the entire detector circuit.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,498,554 to Mei in view of 6,444,487 to Boggs et al.

Incorporating all arguments of Claim 1 and noting that Mei fails to explicitly teach at least one micro-electro-mechanical (MEM) element in the substrate.

However, Boggs et al., in Figures 16-27 and column 3 lines 55-65 and columns 6-7 lines 37-24, teaches a micro-electro-mechanical element within a substrate with CMOS and DMOS technology (i.e. – low and high voltage well implants).

It would have been obvious to one of ordinary skill in the art to modify Mei by incorporating a micro-electro-mechanical element within a substrate with CMOS and

DMOS technology, as taught by Boggs et al., to prevent having to later attach the MEMS device on the substrate which requires high precision instruments.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,498,554 to Mei in view of 6,130,458 to Takagi et al.

Incorporating all arguments of Claim 1 and noting that Mei fails to explicitly teach wherein providing a substrate comprises providing a silicon on insulator wafer comprising a single crystal silicon layer, a substrate and an insulator layer therebetween.

However, Takagi et al., in Figures 5A and 10B and columns 3-4 lines 15-28 and column 6-10 lines 30-64, teaches a substrate comprised by a silicon on insulator wafer with a single crystal silicon layer, a substrate and an insulator layer therebetween.

It would have been obvious to one of ordinary skill in the art to modify Mei by incorporating a substrate comprised by a silicon on insulator wafer with a single crystal silicon layer, a substrate and an insulator layer therebetween, as taught by Takagi et al., to prevent the formation of inversion layers which can cause leakage currents.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,498,554 to Mei in view of 6,130,458 to Takagi et al.

Incorporating all arguments of Claims 1 and 6 and noting that Mei fails to explicitly teach wherein providing a substrate comprises providing a silicon on insulator wafer comprising a p-type silicon layer, a substrate and an insulator layer therebetween.

However, Takagi et al., in Figure 10B and columns 3-4 lines 15-28 and column 6-10 lines 30-64, teaches a substrate comprised by a silicon on insulator wafer with a p-type silicon layer, a substrate and an insulator layer therebetween.

It would have been obvious to one of ordinary skill in the art to modify Mei by incorporating a substrate comprised by a silicon on insulator wafer with a p-type silicon layer, a substrate and an insulator layer therebetween, as taught by Takagi et al., to prevent the formation of inversion layers which can cause leakage currents.

10. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over 6,258,701 to Depetro et al. in view of 5,498,554 to Mei.

Depetro et al. teaches providing a silicon substrate (11); forming a first protective layer (12) over the substrate; removing a portion of the first protective layer to expose a first portion (14) of the substrate; creating a first low voltage component (14) of a first circuit device in the first portion of the substrate using the partially removed first protective layer; forming a second protective layer (17) over at least the first portion of

the substrate; removing a second portion of the first protective layer (18) to expose a second portion of the substrate; and creating a high voltage component (18) of a second circuit device in the second portion of the substrate using the partially removed first protective layer (12) and the second protective layer (17). (See Figure 3 and columns 3-4 lines 40-35)

Depetro et al. fails to explicitly teach ion implanting a high voltage well and a first low voltage well.

However, Mei, in columns 3-5 lines 65-30, teaches ion implanting a high voltage well and a first low voltage well.

It would have been obvious to one of ordinary skill in the art to modify Depetro et al. by incorporating ion implanting a high voltage well and a first low voltage well, as taught by Mei, to achieve precise control of dopant concentration and dopant uniformity.

Allowable Subject Matter

11. Claims 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach, in combination with the other claimed features, forming a sixth protective layer over at least the field oxide layer and the

polysilicon gates; removing a portion of the sixth protective layer; and ion implanting at least one P+ source/drain in the P-body and in the first low voltage well of the second circuit device using the partially removed sixth protective layer.

Response to Arguments

Applicant's arguments, see pages 1 and 2, filed February 5, 2004, with respect to the rejection(s) of claim(s) 1-16 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of 5,498,554 to Mei and other cited art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (571) 272-1691. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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